

No. of Pages: 02

Roll No:

A-06

B. Tech. CSE-AIDS/AIML/CS Ist Semester Examinations (Dec. 2025)
Basics of Electronics Engineering (BT-ECE-101A)

Time: 3hrs

Max. Marks: 60

Attempt 5 questions in all, selecting one question from each unit, however, Question 1 is compulsory. Each full Question carries 12 marks.

Q.1	Marks
(a) Define active and passive components, cite at least one example of active component and at least three examples of passive components.	2
(b) How many minimum number of diodes are required to make a full wave rectifier (with or without any other necessary machine or apparatus, etc.)? Draw a diagram of such a full-wave rectifier connected to supply source and some load.	2
(c) How can a transistor be used as a switch? What are the two properties of switch that are satisfied by a transistor? In what mode(s) of operation of the transistor, these properties come into play?	2
(d) Define alpha, beta and gamma for a transistor. What are the relationship(s) amongst them?	2
(e) A single hex digit has how many possible values? Those values range from what to what in hexadecimal and in decimal? A two-digit hex number has how many possible values? Those values range from what to what in hexadecimal and in decimal?	2
(f) What are universal gates? Why these are so called?	2
UNIT-I	
Q.2(a) What are the distinctions (distinct features / characteristics), if any, among the Zener Diode, Avalanche diode, and Schottky diode?	6
Q.2(b) Draw a voltage regulator using Zener Diode, showing all essential components (besides Zener diode too), supply and load (if any). Illustrate its working. Against changes in what, does it regulate?	6
Q.3(a) Is solar cell different from Photovoltaic cell? Describe the construction and working of Photovoltaic cell. What are its applications?	6
Q.3(b) Explain the construction & working of a PN junction. Plot its V-I characteristics.	6
UNIT-II	
Q.4(a) Draw a circuit (along with supply source and a load) of Common Collector Configuration of an NPN transistor and explain its working. Draw its Input and Output characteristics also.	9
Q.4(b) What is the main purpose of a common collector transistor amplifier?	3

- Q.5(a) Draw a typical load line and the relevant characteristics of a transistor to demonstrate the choice of operating point of a transistor. What is the main advantage of choosing a proper operating point? What happens if the operating point is not properly chosen? 7
- Q.5(b) Compare three configurations (CB, CE & CC) of transistor amplifier based on input & output resistances (or impedances), current and or voltage gains (as applicable), etc. 5

UNIT-III

- Q.6(a) Perform the following binary arithmetic operations: 8
 $1010 + 1100$; $1110 + 1011$; $1111 - 1010$; $1011 - 110$.
- Q.6(b) Write the procedure to convert binary numbers to Gray codes. 4
- Q.7(a) Convert the Gray codes 1010 and 1101 into corresponding binary numbers. 7
- Q.7(b) Convert the decimal numbers 456 and 279 to BCD and then perform their addition in BCD. Show the result in BCD and decimal 5

UNIT-IV

- Q.8(a) Draw a logic circuit to implement the Boolean expression $C = A' B + A B'$ using basic logic gates. Also explain the working of the circuit. 8
- Q.8(b) What is a canonical form of expression? Give an example. What are min terms? 4
- Q.9(a) Using Boolean algebra theorems, simplify the following expression: 7
 $F = A + A' B$
- Q.9(b) Write a short note on LCD. 5

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Roll No.....

A-09

**B. Tech. CE/CSE/ME/TE/ECE/IT I/II Semester Examinations (Dec 2025)
Basics of Electrical & Electronics Engineering (BT-ECE-102A)**

Time - 03hrs

Max. Marks - 60

*Attempt 5 questions in all, selecting one question from each unit and Question 1 is compulsory.
Each Question carries 12 marks.*

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|--------|---|----|
| Q1.(a) | Draw a well labeled electrical circuit diagram with R, L, and C and current source. | 02 |
| Q1.(b) | Define Delta-Star conversion. | 02 |
| Q1.(c) | Compare the reactive & apparent powers. | 02 |
| Q1.(d) | Discuss the basic principle of Emf equation. | 02 |
| Q1.(e) | What do you mean by breakdown in PN diode? | 02 |
| Q1.(f) | Explain the basic rectifier circuit. | 02 |

Unit 1

- | | | |
|--------|---|----|
| Q2.(a) | Draw and explain the working of Thevenin's Theorem. | 06 |
| Q2.(b) | Explain the working of Schottky diode. | 06 |
| Q3.(a) | Describe the key principles of duality in circuit analysis and synthesis. | 06 |
| Q3.(b) | Draw and explain the working of Star to Delta conversion. | 06 |

Unit 2

- | | | |
|--------|--|----|
| Q4.(a) | Explain the rectangular forms of representation of phasor quantities in AC circuits. | 06 |
| Q4.(b) | Draw and explain the Steady-state AC response of RC series circuit. | 06 |
| Q5.(a) | Discuss the subtraction of two sinusoidal quantities using the component resolution method/ phasors. | 06 |
| Q5.(b) | Draw and explain the Steady-state AC response of RLC parallel circuit. | 06 |

Unit 3

- | | | |
|--------|--|----|
| Q6.(a) | Mention the various types and causes of transformer losses. Explain the difference between hysteresis and eddy current losses. | 06 |
| Q6.(b) | How to reduce the iron and copper loss in the transformer? Explain | 06 |
| Q7.(a) | Explain the braking of dc motors. | 06 |
| Q7.(b) | Describe the various four quadrant operation of DC motor with applications. | 06 |

Unit 4

- | | | |
|--------|--|----|
| Q8.(a) | Explain the VI characteristics of an ideal diode. Also describe the diode equation. | 06 |
| Q8.(b) | In a transistor circuit, collector load is $4K\Omega$ whereas quiescent collector current is 2mA. Given $V_{CC} = 20V$, determine the operating point and calculate the base current and alpha assuming $\beta = 200$ | 06 |
-

Q9.(a) With the help of a circuit diagram show that a transistor can act like an amplifier. **06**

Q9.(b) In a transistor circuit, the collector load resistor is $R_C=6.3 \text{ K}\Omega$, and $V_{CC}=15 \text{ V}$. **06**
The transistor has a $\alpha = 0.79$, and the base current $I_B=40 \mu\text{A}$. Find the collector current, collector-emitter voltage and emitter current

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C-91

B. Tech. Electronics & Communication Engineering III Semester Examinations (Dec 2025)
Signals & Systems (BT-ECE-201A)

Time- 3hrs

Max.Marks-60

Attempt 5 questions in all, selecting one question from each unit and Question 1 is compulsory. Each Question carries 12 marks.

Q.1	Marks
(a) Define unit step and ramp signal.	2
(b) What is the difference between continuous-time and discrete-time signals?	2
(c) Define transfer function.	2
(d) Write the statement of sampling theorem.	2
(e) Explain the term "Region of Convergence" in Laplace Transform.	2
(f) Write the final value theorem for z transform.	2

UNIT-I

Q.2(a) Determine the range of values 'a' and 'b', for which the LTI system with impulse response $h(n) = \begin{cases} a^n, n \geq 0 \\ b^n, n < 0 \end{cases}$ is stable	9
Q.2(b) Compare static with dynamic system.	3
Q.3(a) Prove that convolution in the time domain corresponds to multiplication in the frequency domain. Explain its physical significance.	9
Q.3(b) Compare stable with unstable system	3

UNIT-II

Q.4(a) Determine the Fourier transform of a rectangular pulse of amplitude A and time duration T.	7
Q.4(b) Determine the inverse Fourier transform of 1. $u(w)$ 2. $\text{sgn}(w)$	5
Q.5(a) Define autocorrelation. State its various properties.	6
Q.5(b) Show that a Dirac comb is its own Fourier transform.	6

UNIT-III

Q.6(a) Explain the concept of aliasing and show how it affects sampled signals.	6
Q.6(b) Derive and explain the Laplace Transform from the Fourier Transform.	6
Q.7(a) Discuss the properties of Laplace Transform and its applications.	9
Q.7(b) Define poles, zeros and system stability.	3

UNIT-IV

Q.8(a) What is the utility of Fourier and Z- transform? Derive the relationship between the two.	8
Q.8(b) Explain the significance of ROC in Z-transform.	4
Q.9(a) Determine the inverse z-transform of $X(z) = \frac{1}{(z-0.25)(z-0.5)}$, ROC : $ z >0.5$	8
Q.9(b) Explain the initial and final value theorem for Z-transform.	4

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C-92

**B. Tech. Electronics & Communication Engineering III Semester Examinations (Dec 2025)
Electronic Devices & Circuits (BT-ECE-203A)**

**Time- 3hrs
Max.Marks-60**

Attempt 5 questions in all, selecting one question from each unit and Question 1 is compulsory. Each Question carries 12 marks.

Q.1	Marks
(a) Compare Intrinsic and Extrinsic semiconductors. Explain why can't we add divalent and hexavalent impurity to intrinsic semiconductors to make it extrinsic semiconductor.	
(b) Compare the parameters of CB, CE and CC configurations of a transistor.	
(c) Explain the Bias compensation method with the help of a diode.	
(d) Compare BJT and FET.	
(e) Why do we need biasing?	
(f) How negative feedback improves the stabilization.	
UNIT-I	
Q.2(a) State and explain drift and diffusion current mechanism in semiconductors. Derive an expression for the potential barrier in PN Junction diode.	6
Q.2(b) Explain the concept of Continuity equation. Derive an expression for the movement of charges within the semiconductor.	6
Q.3(a) What is clamping? Draw the circuits and waveforms for positive and negative clampers.	6
Q.3(b) Explain the working of Tunnel Diode. Draw its characteristics and explain its different regions of working.	6
UNIT-II	
Q.4(a) What are the various current amplification parameters of a transistor in CE, CB and CC configuration? Derive expression for each component and also fetch a relation among them.	6
Q.4(b) What is Eber's Moll Model of a transistor? Explain how transistor model is justified by Eber and Moll?	6
Q.5(a) Derive an expression for current gain, voltage gain, input impedance for C.E configuration using hybrid model.	6
Q.5(b) State and Explain Non-Ideal effects of transistor. Explain each effect with suitable diagram.	6

UNIT-III

- Q.6(a) Draw and explain the structure of N- Channel depletion type MOSFET. Explain its working while drawing its characteristics and mention various area of it. 6
- Q.6(b) Draw the small signal model of MOSFET and explain its different design parameters in detail. 6
- Q.7 Write Short Notes on: 6 x 2
- (a) Shockley Equation
 - (b) MOS Capacitor

UNIT-IV

- Q.8(a) Draw and explain the concept of biasing. How Self bias is used to re-fix the operating point at its original position if deviated due to any of the reason? 6
- Q.8(b) How thermal Runaway can be avoided? Derive a mathematical relationship among the voltage and current components which saves the burning out of the collector junction. 6
- Q.9 Derive Gain with Feedback, I/p and o/p resistances with feedback for the following topologies. Also draw their equivalent electronic circuits for both of them and compare with the block diagrams of the feedback topologies. 6x2
- (a) Current Series Feedback topology
 - (b) Voltage shunt feedback topology

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C-93

B. Tech. Electronics & Communication Engineering III Semester Examinations (Dec 2025)
Digital System Design (BT-ECE-205A)

Time- 3hrs

Max.Marks-60

Attempt 5 questions in all, selecting one question from each unit and Question 1 is compulsory. Each Question carries 12 marks.

Q.1	Marks
(a) What is a universal gate? Name its types with its truth table.	2
(b) Describe how an 8-bit binary number is converted to Gray code.	2
(c) Elaborate on Quine-McCluskey simplification method.	2
(d) Define a T flip flop with its logic symbol and truth table.	2
(e) Discuss various characteristics of logic families.	2
(f) Discuss the specifications of Digital to Analog converters.	2

UNIT-I

Q.2(a) What is TTL? Explain with suitable diagrams.	8
Q.2(b) Discuss the Excess3 code. Convert 99 to its equivalent Excess-3 code.	4
Q.3(a) Explain tri state logic and its significance.	6
Q.3(b) Perform the following subtraction using 1's complement arithmetic: $(11010)_2 - (01101)_2$	6

UNIT-II

Q.4(a) Design a full adder with its truth table and circuit using suitable logic gates.	6
Q.4(b) Solve the following expression using K-Map $Y(A,B,C) = \sum m(0,1,3,5)$	6
Q.5(a) What is a demultiplexer? Draw and explain the working of a 1:8 demultiplexer.	4
Q.5(b) Design a 7 segment to BCD decoder.	8

UNIT-III

Q.6(a) Draw and explain Mod5 asynchronous counter using JK flip flops.	8
Q.6(b) What is a flip-flop. Discuss the applications of flip-flops.	4
Q.7(a) Explain the working of D flip flop with its logic symbol and truth table.	6
Q.7(b) Explain the working of 4 bit SISO register using D flip flops.	6

UNIT-IV

Q.8(a) Discuss the working of a R-2R ladder Digital to Analog converter.	8
Q.8(b) Elaborate on the specifications of Analog to Digital converters	4
Q.9(a) Draw and explain the working principle of PAL. Discuss how it differs from PLA.	8
Q.9(b) Differentiate between RAM and ROM.	4

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B. Tech. Electronics & Communication Engineering III Semester Examinations (Dec 2025)
Network Analysis & Synthesis (BT-ECE-207A)

Time- 3hrs

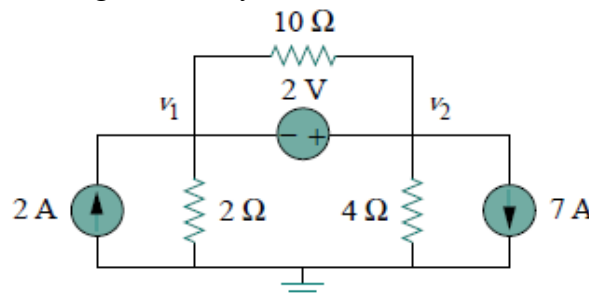
Max.Marks-60

Attempt 5 questions in all, selecting one question from each unit and Question 1 is compulsory. Each Question carries 12 marks.

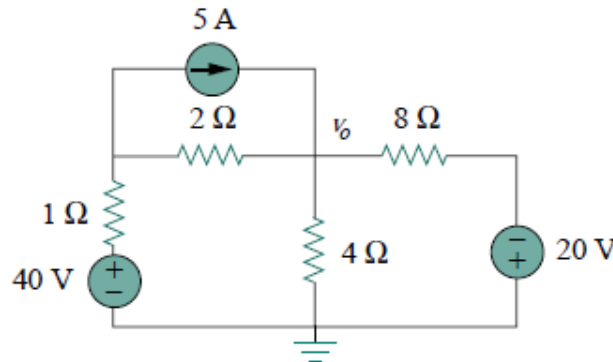
Q.1	Marks
(a) Define active and passive components with example.	2
(b) Explain KCL with Example.	2
(c) Define Transfer function of a network.	2
(d) Define cut-off frequency of a filter.	2
(e) Define poles and zeros in network functions.	2
(f) Write the significance of Hurwitz polynomials in network synthesis	2

UNIT-I

Q.2(a) Determine v_1 and v_2 using node analysis in the circuit shown in following Fig. 6



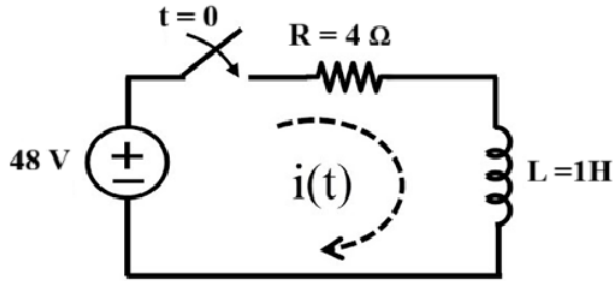
Q.2(b) Apply mesh analysis to find v_o in the following circuit. 6



Q.3(a) Describe the following terminology in graph theory. 6

- (i) Node (ii) Tree (iii) Twig (iv) Co-Tree (v) Loop (vi) Mesh

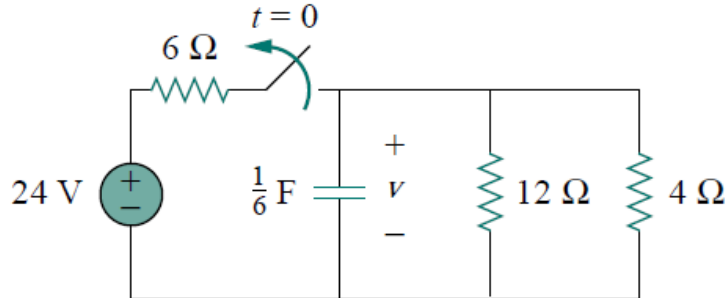
Q.3(b) Determine the current $i(t)$ for $t \geq 0$ in the following RL circuit using Laplace transform. Assume that the initial current through inductor is 3A. 6



UNIT-II

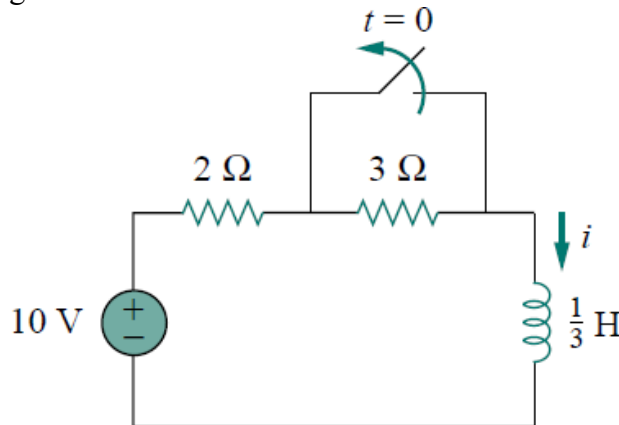
Q.4(a) Determine $v(t)$ for $t \geq 0$ in the following circuit.

6



Q.4(b) Find $i(t)$ in the following circuit for $t > 0$. Assume that the switch has been closed for a long time.

6

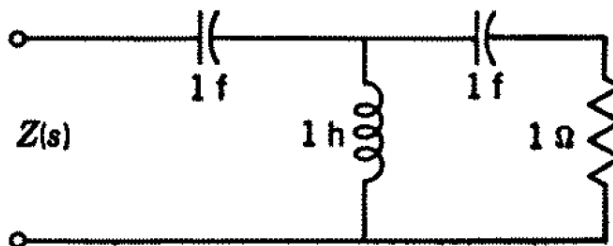


Q.5(a) Explain how the location of poles in the s-plane affects the stability and time-domain response of a network. Illustrate with examples of poles on left half, right half and $j\omega$ -axis.

6

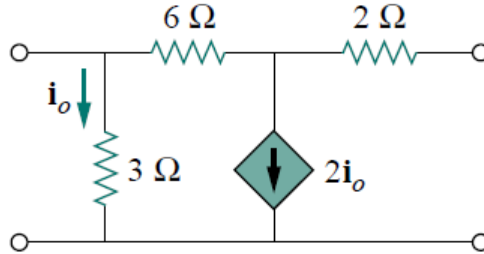
Q.5(b) Find the driving-point impedance for the network shown in below Fig. Arrange the polynomials of this function with the high ordered term normalized to unity coefficient.

6



UNIT-III

Q.6(a) Identify the y parameters for the circuit given in below Fig. 6



Q.6(b) Obtain the h parameters from the given Z parameters for a two-port network. 6

Q.7(a) Draw and describe the basic structure of a constant- k high-pass filter. What components determine its cutoff frequency? 6

Q.7(b) Illustrate the low pass filter. Derive the transfer function for low pass filter and plot the frequency response curve. 6

UNIT-IV

Q.8(a) Test whether the polynomial $P(s) = s^3 + 4s^2 + 5s + 2$ is Hurwitz or not. 6

Q.8(b) Test whether $F(s) = \frac{s^2+6s+5}{s^2+9s+14}$ is positive real function or not. 6

Q.9(a) Realise Cauer II form of the function 6

$$F(s) = \frac{s(s^4 + 3s^2 + 1)}{3s^4 + 4s^2 + 1}$$

Q.9(b) Realise the Foster I forms of the following impedance function. 6

$$F(s) = \frac{4(s^2 + 1)(s^2 + 9)}{s(s^2 + 4)}$$

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C-95

B. Tech. Electronics & Communication Engineering III Semester Examinations (Dec 2025)
Analog Communication (BT-ECE-209A)

Time- 3hrs

Max.Marks-60

Attempt 5 questions in all, selecting one question from each unit and Question 1 is compulsory. Each Question carries 12 marks.

Q.1	Marks
(a) State Quadrature Null Effect and warble.	2
(b) Find the modulation index of a frequency modulated signal having frequency deviation 50 kHz and maximum message frequency is 500 Hz.	2
(c) Write the Fourier transform of A (Constant).	2
(d) Define term White Noise.	2
(e) Define the bandwidth for FM Carson's Rule	2
(f) Determine the instantaneous angular velocity of a wave having a total phase angle given by, $\Psi(t)=2000t + \sin 10t$.	2

UNIT-I

Q.2(a) Describe the block diagram of digital communication and compare it with analog communication.	6
Q.2(b) Explain the classification of noise in communication systems. Discuss characteristics and sources of thermal noise, shot noise, flicker noise, and tr time noise with suitable mathematical expressions.	6
Q.3(a) Discuss the transmission of noise through linear systems. Define signal-to-ratio (SNR), noise bandwidth, and explain how system bandwidth affects power at the output of a filter or amplifier.	6
Q.3(b) Explain classification of Modulation Schemes based on carrier and modulating signal.	6

UNIT-II

Q.4(a) Explain envelope detection of AM Wave with help of characteristics diagram.	6
Q.4(b) A certain transmitter radiates 9 kW with the carrier unmodulated, and 10.125 kW when the carrier is sinusoidally modulated. Calculate the modulation index. If another sine wave, corresponding to 40 percent modulation, is transmitted simultaneously, determine the total radiated power.	6
Q.5(a) Write a short note on Single Side band-Suppressed Carrier (SSB-SC) and explain its advantages as well as disadvantages.	6
Q.5(b) Explain the critical modulation, over modulation and under modulation w.r.t. modulation index of AM Wave.	6

UNIT-III

- Q.6(a) Demonstrate Narrow Band Frequency Modulation with mathematical expression. 6
- Q.6(b) Consider an angle modulated signal $x(t) = 5\cos[2\pi 10^6 t + 5\sin(2\pi t)]$. Find its 6
- (a) Instantaneous frequency at time $t=0.5\text{ms}$, $t=0.75\text{ms}$.
- (b) Maximum phase deviation. (c) Maximum frequency deviation
- Q.7(a) Illustrate the relation between the transfer function of Pre-emphasis and De-emphasis for frequency modulation. 6
- Q.7(b) Develop a general expression of PM wave. Obtain the value of modulation index and find the bandwidth when, 6
- (a) f_m ,
- (b) f_m is decreased by one-half.
- The required data is given as below.
- Consider an angle modulated signal $x_c(t) = 10 \cos(\omega_c t + 5 \sin \omega_m t)$. Assume it a PM and $f_m = 1 \text{ kHz}$.

UNIT-IV

- Q.8(a) Describe the construction and working principle of an Armstrong FM transmitter. Explain how phase modulation is converted into frequency modulation. 6
- Q.8(b) With the help of diagrams, explain image signal rejection, frequency mixers, IF selection, and the importance of tracking and alignment in superheterodyne receivers. 6
- Q.9(a) Define frequency scintillation and frequency drift. Explain their causes, effects on radio communication, and methods used to minimize them. 6
- Q.9(b) Draw and describe the block diagram of an AM transmitter. Explain the role of each stage in details. 6

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No. of Pages: 02

Roll No:

C-422
BBA(DM) III Semester Examinations (Dec 2025)
Internet of Things & Google Ads (BT-ECE-219A)

Time- 3hrs
Max.Marks-60

Attempt 5 questions in all, selecting one question from each unit and Question 1 is compulsory. Each Question carries 12 marks.

Q.1	Marks
(a) Differentiate between the physical design and logical design of the Internet of Things (IoT).	2
(b) List any four applications of IoT in real life.	2
(c) Define RFID and mention any two of its applications.	2
(d) List any two types of campaign formats available in Google Ads and write one line on each.	2
(e) Write the correct Google Ads account hierarchy.	2
(f) What is a responsive ad in Google Ads? How is it different from a text ad?	2

UNIT-I

Q.2(a) Define the Internet of Things (IoT). Explain any four major characteristics of IoT with suitable examples.	6
Q.2(b) Describe the history and evolution of IoT from M2M communication to advanced smart systems.	6

OR

Q.3(a) Explain IoT architecture in detail with suitable diagram.	6
Q.3(b) How is edge computing used in IoT?	6

UNIT-II

Q.4(a) Describe the applications of sensors in everyday activities.	6
Q.4(b) What are actuators? Classify them with suitable examples and write any two use cases.	6

OR

Q.5(a) Write a note on the Arduino board, highlighting its features and uses in IoT.	6
Q.5(b) Explain the concept of Wireless Sensor Networks (WSN) and discuss their components.	6

UNIT-III

Q.6(a) What are Video Campaigns in Google Ads? Discuss different types of video ads and their importance in digital marketing.	6
Q.6(b) Explain App Campaigns and Shopping Campaigns in Google Ads. Highlight the goals and industries where each is most suitable.	6

OR

- Q.7(a) Discuss how Google Ads helps in achieving different digital marketing goals such as brand awareness, lead generation and sales with suitable examples. **6**
- Q.7(b) Write a detailed note on the role of Google Ads in a business's digital strategy. How does it support targeting, remarketing, analytics, and budget control? **6**

UNIT-IV

- Q.8(a) What are Negative Keywords? Explain their importance with examples. **6**
- Q.8(b) What is Manual CPC and Target CPA bidding? Compare both methods. **6**

OR

- Q.9(a) Discuss any two ad extensions like Sitelink, Callout, or Structured Snippets and give examples. **6**
- Q.9(b) What is meant by campaign optimization in Google Ads? Give short notes on Quality Score and Performance Reports. **6**

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Roll No:

C-12

B. Tech CSE/Information Technology III Semester Examinations (Dec 2025)

Digital System Design (BT-ECE-221A)

Time- 3hrs

Max.Marks-60

Attempt 5 questions in all, selecting one question from each unit and Question 1 is compulsory. Each Question carries 12 marks.

Q.1	Marks
(a) State De Morgan's laws	2
(b) Convert 36.25 into Octal	2
(c) Define a combinational circuit.	2
(d) Differentiate between a latch and a flip flop.	2
(e) Discuss the specifications for DACs.	2
(f) Distinguish between RAM and ROM.	2

UNIT-I

Q.2(a) Perform the following binary subtractions using the 2's complement method: $(1101)_2 - (1011)_2$ Given the Boolean expression	6
Q.2(b) $f(a,b,c) = (a'b + c)(b+c')$ simplify it using Boolean algebra.	6
Q.3(a) Minimize the following expression using K-Map: $Y(A,B,C,D) = \sum m(1,3,5,7,9,15) + d(2,4)$	8
Q.3(b) What is a Product of Sums (POS) form? How does it differ from a Sum of Products (SOP) form?	4

UNIT-II

Q.4(a) Design a half subtractor using suitable logic gates.	4
Q.4(b) Design a BCD to 7 Segment encoder with suitable logic gates.	8
Q.5(a) Design a 2-bit magnitude comparator using the Boolean expressions derived from its truth table.	6
Q.5(b) Implement the following expression using a suitable multiplexer: $Y(A,B,C,D) = \sum m(1,3,4,5,7,9)$	6

UNIT-III

Q.6(a) Draw and explain Asynchronous Decade Counter using D flip flops.	6
Q.6(b) Explain the "forbidden state" (or invalid condition) in an SR latch and why it is not suitable.	6
Q.7(a) Convert a T Flip-Flop from a JK Flip-Flop.	6
Q.7(b) Explain the operation of a 4 bit Bi-directional Shift Register with suitable diagrams.	6

UNIT-IV

Q.8(a)	How can EEPROM be programmed and erased?	6
Q.8(b)	Discuss the implementation of a PAL using a ROM.	6
Q.9(a)	How does an R-2R ladder DAC overcome the disadvantages of a weighted resistor DAC?	8
Q.9(b)	Elaborate on specifications for an ADC.	4

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Roll No:

C-35

B. Tech. CSE-AIML/AIDS/CYS III Semester Examinations (Dec 2025)

Digital System Design (BT-ECE-223A)

Time- 3hrs

Max.Marks-60

Attempt 5 questions in all, selecting one question from each unit and Question 1 is compulsory. Each Question carries 12 marks.

Q.1	Marks
(a) Explain the working of NOT, AND and OR gates with its truth table.	2
(b) Distinguish between combinational and sequential circuits.	2
(c) What is a don't care condition? How it is represented in simplification?	2
(d) Elaborate on the process of inter conversion of Flip flops.	2
(e) Define a shift register. State its types with suitable diagrams.	2
(f) Define programmable logical device. Mention its types.	2
UNIT-I	
Q.2(a) Construct all the gates using NAND gates only.	6
Q.2(b) Design a half subtractor with suitable gates and logic.	6
Q.3(a) Construct an 8:1 MUX using 4:1 MUXs.	4
Q.3(b) Design a BCD adder.	8
UNIT-II	
Q.4(a) Define a flip flop. State its applications.	4
Q.4(b) Draw and explain the working of Master Slave JK flip flop.	8
Q.5(a) Explain the working of SIPO shift register using D flip flops.	6
Q.5(b) Design a Mod 6 asynchronous counter using JK flip flops.	6
UNIT-III	
Q.6(a) Distinguish between parity checker and parity generator.	6
Q.6(b) Elaborate on magnitude comparator with a suitable example.	6
Q.7(a) Discuss the analog to digital conversion using dual slope ADC.	8
Q.7(b) Describe the specifications of Digital to Analog converters.	4
UNIT-IV	
Q.8(a) Differentiate between PROM, EPROM, EEPROM, and EAPROM.	6
Q.8(b) Draw the architecture of a Programmable Logic Array (PLA) and Programmable Array Logic (PAL). State the differences in their programmability and circuit structure.	6
Q.9(a) Implement a ROM using PLAs.	8
Q.9(b) Describe the classification of memory.	4
